PATENT
8008-1052

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re application of

Yasutaka NAKASHIBA	Conf. 2273
Application No. 10/812,282	Group 2815
Filed March 30, 2004	Examiner Jerome Jackson Jr.

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

May 18, 2010

Sir:

In compliance with Rules 1.97 and 1.98, and in fulfillment of the duty of disclosure under Rule 1.56, the accompanying documents, copies of which are attached to this statement, are made of record on the enclosed Form PTO-1449.

A concise explanation of the relevance of these items is that these references were cited by the Japanese Patent Office in the corresponding Japanese Application Serial No. 2003-106118, dated March 23, 2010. A copy of the Japanese Official Action in which they were cited is attached hereto, with what is believed to be the pertinent portion enclosed in a wavy line. An English translation of the enclosed portion is also attached hereto.

Under the provisions of 37 CFR 1.97(e), the undersigned hereby certifies that each item of information contained in this Information Disclosure Statement was first

cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Statement.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future submissions, to charge any underpayment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

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